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Power Reduction and Glitch free MUX based Digitally Controlled Delay-Lines

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ABSTRACT : *A wide range MUX based Digitally Controlled Delay Line (DCDL) is presented to achieve low jitter, low power and process immunity. The proposed DCDL have been designed in 90 nm CMOS technology. The proposed MUX based DCDL maintains the same resolution and minimum delay of NAND-based DCDL. In this paper the theoretical demonstration of the glitch-free operation of proposed DCDL is derived. Simulation result shows that novel circuits result in the lowest resolution, with a little worsening of the minimum delay with respect to the previously proposed DCDL with lowest delay. The NAND based DCDL avoid the glitching problem, but the power consumption rate and area will be increased. The proposed MUX based DCDL. Which overcome the limitation by NAND based DCDL.*

Keywords- **All** ***–digital delay locked loop (ADDLL), all – digital phase locked loop (ADPLL), Control code word, Digitally controlled delay lines (DCDL), Delay –Line.***

1. INTRODUCTION

In recent deep-sub micrometer CMOS processes, voltage resolution of analog signals is becoming lower than time-domain resolution of a digital signal. This claim is now a day's pushing toward a new circuit design paradigm in which the traditional analog signal processing is expected to be progressively substituted by the processing of times in the digital domain. Digitally controlled delay lines (DCDL) should play the role of digital-to-analog converters in analog-intensive, circuits traditionally. From a more practical point of view, nowadays, DCDLs are a key block and it has number of applications, like all-digital PLL (ADPLL), all-digital DLL (ADDLL), all-digital spread-spectrum clock generators (SSCGs).

By using a regular cascade of equal delay element (DE), DCDL is constructed. Each delay element is constructed by using only NAND gates it is obtained a very good linearity and resolution. The method is by using three – state inverters (TINV). Here each delay element is constructed by using three
state inverters, obtains a resolution $t_r = 2t_{TINV}$. The other method is DCDL constructed using inverter and an inverting multiplexer. This INVERTER+ MUX topology, presents two drawbacks. A first drawback is due to the different delays of the inverter and the multiplexer which results in a mismatch between odd and even Control-codes. This mismatch results in an increased INL. A second drawback is due to the large multiplexer delay.

A common design problem in systems employing DCDLs is glitching. The DCDLs are employed to process the clock signals in most case; therefore a glitch-free operation is required. A necessary condition is to avoid glitching, to set delay control-code switching. This is an issue at the DCDL-design level. Many approaches are known to avoid glitching in MUX-based DCDLs [8]–[10].

In these topologies glitching can be avoided by using a thermometer code for the control-bits. The NAND-based DCDL topology [3]–[6] presents a glitching problem. It is worth to note that in the ADDLL topologies of [3]–[6] the DCDL glitching is filtered by the phase detector and harmonic locking circuitry during locking phase. In other applications, however, the presence of this glitching phenomenon can substantially limit the employ of NAND-based DCDLs.

The design of NAND based DCDL has two contributions. First it is shown and analyzed the glitching problem of the NAND-based DCDL of [3]–[6]. Afterwards a novel glitch-free NAND-based DCDL is presented. The proposed NAND-based DCDL allows achieving a resolution similarly to the NAND-based DCDL of [3]–[6]. The NAND based DCDL avoid the glitching problem but the area and power consumption rate will be increased. This paper proposes MUX based DCDL which reduces the glitching problem and also reduces the power consumption rate.

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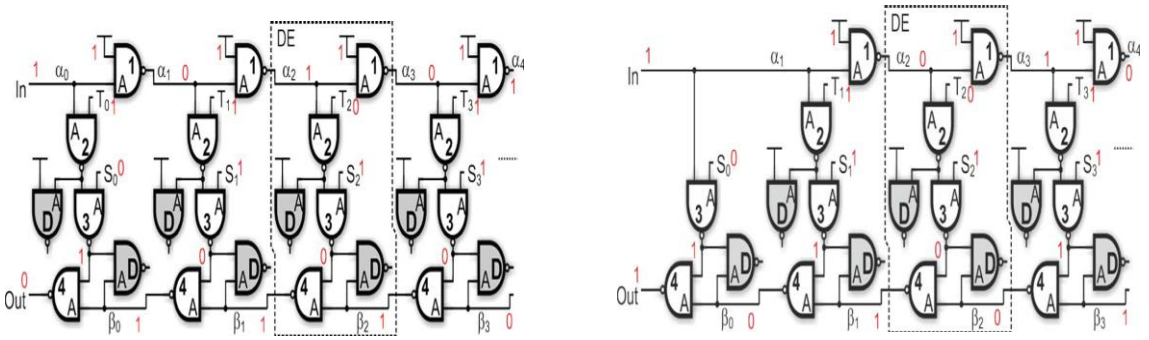
II.NAND-BASED DCDL AND GLITCHING

The structure of NAND based DCDL is shown in Fig.1. The circuit is composed by a series of equal delay elements, each elements is composed by NAND gates. In this figure "A" denotes the fast input of each NAND gate. Gates marked with "D" represents dummy cells [1]-[2] it is added for load balancing. The two sets of control-bits s_i and t_i, control the DCDL.To avoid DCDL output glitching; the switching of delay control-bits is synchronized with the switching of *In* input signal.

There are three possible driving circuits for the control- bits of proposed DCDL.Signals delayed with different LH/HL delays and different LH/HL delays by using clock tree delay and double clock flip-flops.



(a) (b)

Fig.1 previously proposed glitch-free NAND-based DCDL: (a) inverting topology, (b) non-inverting topology

Glitching problem can be avoided if the control-bits arrival time is lower than the arrival time of the input signal of the first delay element (DE) which switches from post or to the turn-state. When the control code is increased by more than one, glitching problem can occur. The s_i bits encode the control code 'c' by using a thermometric code: Tc_{+1}=0, Ti=1for i≠c+1. The Fig.1 shows that the state of all signals in the case ln=1, and c=1. According to the chosen control-bits encoding, each delay-element (DE) can be in one of three possible states. That is pass state, Turn state, and post turn state. The delay element with $i < c$ are in pass-state (S_i=0, Ti=1). In this state the NAND "3" output is equal to 1 and the NAND "4" allows the signal propagation in the lower NAND gates chain. The DE with i=c is in turn-state ($S_i = T_i = 1$) . In this state the upper input of the DE is passed to the output of NAND "3". The next DE (i=c+1) is in post-turn-state ($S_i = 1, T_i = 0$) . In this DE the output of the NAND "4" is stuck-at 1, by allowing the propagation, in the previous DE (which is in turn-state), of the output of NAND "3" through NAND "4". All remaining delay element (DE) for (i>c+1) are again in turn-state ($S_i = T_i = 1$).The three possible DE states of proposed DCDL and the corresponding S_i and T_i values are summarized in Table I.

TABLE I
Logic state of each DE in proposed DCDL

S_i	T_i	DE state
0	1	Pass
1	1	Turn
1	0	Post- Turn

In the proposed DCDL the state of all α_i and β_i signals depends on the input ($\alpha_{2i=\beta_{2i}} = \ln$ and $\alpha_{2i=\beta_{2i}} = \ln-$) with the only exception of β_c , which is stuck-at 1. The glitch-free switching property of the proposed DCDL is conceptually simple to demonstrate. Let us assume a switching of the delay control-code

from c= k to c= h. In the initial state of the line, $\alpha_{2i=\beta_{2i}} = 1n$ and $\alpha_{2i=\beta_{2i}} = 1n -$ with the exception of β_k, Let us suppose to first switch the k+1 th DE.

By looking to Fig 1(b) it can be observed that, in these conditions, β_k switches from 1 to α_k . The signal β_k is the input of the NAND "4" gate of k^{th} DE. The switching of β_k is glitch-free since the other input of this gate is stuck-at α_k, therefore the NAND "4"output remains equal. After the $k+1^{th}$ DE switching, all cells are either in pass-state or in turn-state.

In these conditions it is possible to freely change the state of DEs from pass-state to turn-state, since this change does not affect the logic state of signals and. After this phase $h+1^{th}$ DE can be switched from turn-state to post-turn-state. Since only when the signal β_k switches from α_h to 1. This switching is again glitch free.

III. SWITCHING OF NAND BASED DCDL AND CONTROL-BITS DRIVING CIRCUITS

The NAND based DCDL can be obtained with a three-step switching mechanism: for a switching from a delay control code c= k to c= h a delay control code, first, the k+1 th DE is switched from post-turn-state to the turn-state; the next all DE are switched from pass to turn-state and finally the h+1 th DE is switched to post-turn-state. This switching mechanism presents the drawback of being slow and can result in a not simple driving circuit for the DCDL control-bits.

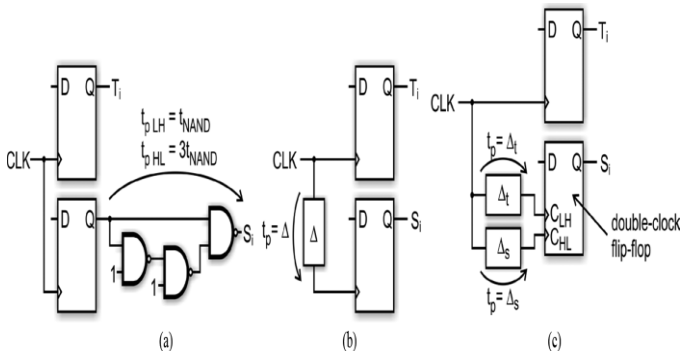


Fig.2 Possible driving circuits for the control-bits of previously proposed DCDL: (a) signals delayed with different LH/HL delays by using a NAND-based circuit; (b) signals delayed using clock-tree delay (c) Si delayed with different LH/HL delays by using clock-tree delay and double-clock flip-flops.

The NAND DCDL, shows that a sufficient condition to achieve a glitch-free operation in previously proposed DCDL is imposing the following two timing constraints:

$$t_{S\,HL} - t_{T\,LH} > t_{NAND} \quad (1)$$

$$t_{T\,HL} - t_{S\,LH} > -t_{NAND} \quad (2)$$

$$\Delta_t = t_{S\,LH} - t_{HL} \quad (3)$$

Where $t_{S\,HL}$,$t_{S\,LH}$,$t_{T\,HL}$ and $t_{T\,HL}$ represents the arrival times of HL and LH switching of and signals, respectively. In order to show how this timing constraint can be, in practice, realized let us define two times, Δ_s and Δ_t .

By using the above definitions, the two timing constraints (2) and (3) becomes

$$\Delta_s > t_{NAND} \quad (4)$$

$$\Delta_t < 3t_{NAND} \quad (5)$$

Fig.2 (a) shows the first driving technique. In this solution each S_i signal is obtained by using a flip-flop followed by a NAND-based circuit which presents different LH and HL propagation delays ($t_{p\,LH} \neq t_{p\,HL}$). In this solution $t_{P\,LH} = t_{NAND}$ while $t_{p\,HL} = 3t_{NAND}$.

$$\Delta_S = 3t_{NAND} \qquad \Delta_t = 3t_{NAND} \tag{6}$$

The two constrains (5) and (6) are therefore verified, both with a timing-margin. A drawback of this solution is the relatively large complexity, since, for each signal, a driving circuit composed of three NAND gates is needed (in addition to the flip-flop). The driving circuit of Fig. 2(b) results simpler than the circuit of Fig. 2(a). In this second solution signals are delayed by delaying the clock signal of the flip-flops.

The clock signal delay can be easily obtained by properly designing the clock-tree. As an example, in a standard-cells design flow based on automatic place and route, a different clock-tree delay can be obtained on a flip-flop by flip-flop bases by using the useful-skew feature of the tools. We will name $\Delta$the delay difference between the clock signals ofS_i.

Flip-flops and T_i flip-flops. Therefore, by recalling the definitions (4), in this case, we have

$$\Delta_s = \Delta_t = \Delta \tag{7}$$

The two constraints (5) and (6), therefore, becomes

$$t_{NAND} < \Delta < 3t_{NAND} \tag{8}$$

The third solution of Fig.3(c) joins the advantages of the two previous solutions. The circuit of Fig.3(c) is based on a special flip-flop that is named double-clock flip-flop. This flip-flop employs two different clock signals: one clock signal (C_{LH}) is used to capture the high logic-state of the D input while another clock signal (C_h) captures the low logic-state of the D input. In the driving circuit of Fig.3(c), this special flip-flop allows to control separately the LH and HL instants of switch of the signals through the delays of the two clock signals (C_{LH}) and (C_{HL}).

The three possible driving circuits that can be used to generate the control-bits of the proposed DCDL are shown in Fig 3. By analyzing Figure 3 it can be noted that signals have to be delayed with respect to signals and that it could be useful to have a different delay for LH and HL transitions. It is also worth to note that, to avoid glitching of the DCDL, S_i and T_i signals must themselves be glitch-free. By following this reasoning, in all presented driving circuits, it is assumed that $T_i$signals are generated as output of flip-flops, which, at the same time, both properly time the DCDL considering system-level aspects, and act as deglitching elements.

IV. PROPOSED MUX BASED DCDL

The structure of proposed MUX based DCDL is shown in Fig.3

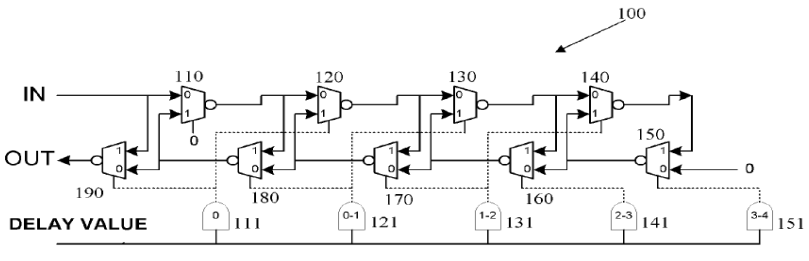


Fig.3. Proposed MUX based DCDL

This present paper relates to the fields of integrated circuit (IC), and more specifically, the present invention relates to programmable delay line circuits with avoidance, and their usage in reconfigurable circuits [11]. A programmable delay line is a circuit where an input signal may be passed to the output of the delay.

Delay line circuits are typically used to adjust the relative delay difference between two signals to achieve reliable data transfer.There may be several disadvantages of the known delay line circuits. On of the potential disadvantage is that most of the known delay line circuit suffer from glitches.

A programmable delay line circuit comprising of the following: first multiplexer having a first input coupled with an input line; second multiplexer having a first input, and a second input coupled with an output of the first multiplexer, and an output coupled with the input of the first multiplexer. A third multiplexer has a first input coupled with the output of the second multiplexer and a second input coupled with an input line, output coupled with the output line. A first control gate is coupled with the third multiplexer to control the third Multiplexer and second control gate coupled with the third multiplexer to control the second multiplexer. The first and second control gates selectively control the third and second multiplexer, in response to a delay value encode in delay to a signal.

V. ANALYSIS AND SIMULATION RESULTS

The schematic diagram and simulated output of the MUX based DCDL is shown in Fig 5 and 6.

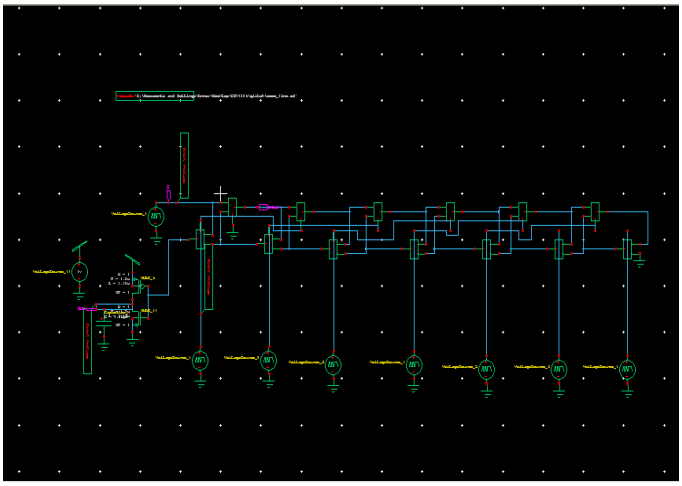


Fig 4. Schematic diagram of MUX based DCDL

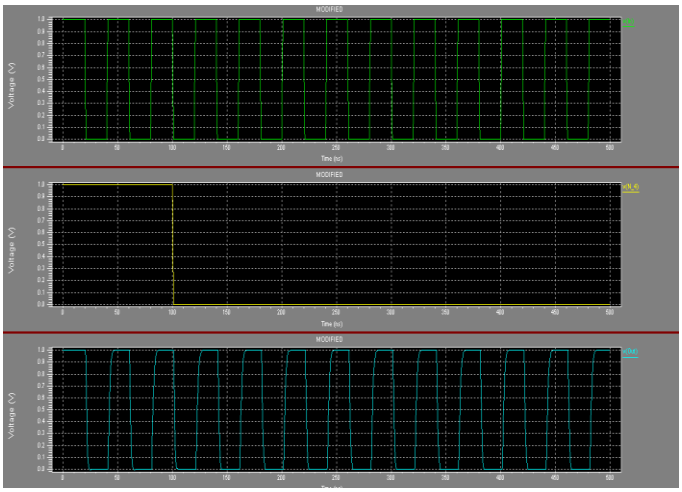


Fig 5. Simulated output of MUX based DCDL

TABLE II

POWER COMPARISON TABLE

TYPES OF DCDL	NAND based DCDL	MUX based DCDL
POWER	7.92 milli watt	3.02 micro watt

VI. CONCLUSION

A NAND-based DCDL which avoids the glitching problem of previous circuit [3]–[6] has been presented. As DCDL structure has been developed to demonstrate the glitch-free property of the proposed circuit. As an additional result, the developed model provides the timing constraints that need to be imposed on the DCDL control-bits in order to guarantee a glitch-free operation. Three different driving circuits for the DCDL control-bits have been considered. In this paper MUX based DCDL is proposed. The simulation results confirm the correctness of developed model and show that proposed solutions improve the resolution with respect to previous approach and also reduce the power consumption rate.

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VIII. REFERENCES

[1]. R. B. Staszewski, K.Muhammad, D. Leipold, "All-digital TX frequency synthesizer and discrete-time receiver for bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, Dec. 2004, vol. 39, no. 12, pp. 2278–229.
[2]. R. B. Staszewski and P. T. Balsara*"All Digital Frequency Synthesizer in Deep Submicron CMOS*" New York: Wiley, 2006.
[3]. R. J. Yang and S. I. Liu, "A 40–550 MHz harmonic-free all digital delay locked loop using a variable SAR algorithm," *IEEE J. Solid-State Circuits*, Feb. 2007, vol. 42, no. 2, pp. 361–37.
[4]. R. J. Yang and S. I. Liu, "A 2.5 GHz all digital delay locked loop in 0.13 mm CMOS technology," *IEEE J. Solid-State Circuits*, Nov. 2007, vol. 42, no. 11, pp. 2338–234.
[5]. S. Kao, B. Chen, and S. Liu, "A 62.5–625-MHz anti reset all digital delay locked loop," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, Jul. 2007,vol. 54, no. 7, pp. 566–57.
[6]. B. M. Moon, Y. J. Park, and D. K. Jeong, "Monotonic wide-range digitally controlled oscillator compensated for supply voltage variation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, Oct. 2008,vol. 55, no. 10, pp. 1036–1040.
[7]. J. A. Tierno, A. V. Rylyakov, and D. J. Friedman, "A wide power supply range, wide tuning range, all static CMOS all digital PLL in 65 nm SOI," *IEEE J. Solid-State Circuits*, Jan. 2008, vol. 43, no. 1, pp. 42–51.
[8]. J. S. Wang, C. Y. Cheng, J. C. Liu, Y. C. Liu, and Y. M. Wang, "A duty cycle distortion tolerant half delay line low-power fast lock in all digital delay locked loop," *IEEE J. Solid-State Circuits*, May 2010,vol. 45, no. 5, pp. 1036–1047.
[9]. T. M. Matano, Y. Takai,Takaishi, H. Fujisawa, S.Kubouchi,"A 1-Gb/s/pin 512-Mb DDRII SDRAM using a digital DLL and a slew-rate-controlled output buffer," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 762–768.
[10]. F. Lin, J. Miller, A. Schoenfeld, M. Ma, and R. J. Baker, "A register controlled symmetrical DLL for double-data-rate DRAM," *IEEE J. Solid-State Circuits*, Apr. 1999, vol. 34, no. 4, pp. 565–568.
[11]. [11] T. Kim, S. H. Wang, and B. Kim, "Fast locking delays-locked loop using initial delay measurement," *Electron. Lett* Aug. 2002, vol. 38, no. 17, pp. 950–951.